WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate including isolation regions and active regions;

a high-k material layer implanted with a species, the high-k material layer proximate the substrate; and

a gate electrode proximate the high-k material layer.

2. The semiconductor device of claim 1, wherein a transistor is formed from the substrate, the high-k material layer, and the gate electrode.

3. The semiconductor device of claim 1, further comprising:

a pre-gate material layer between the substrate and the high-k material layer.

4. The semiconductor device of claim 3, wherein the pre-gate material layer comprises one of SiO_2 and SiON.

5. The semiconductor device of claim 3, wherein the pre-gate material layer has a thickness within the range of 2Å to 10Å.

6. The semiconductor device of claim 1, further comprising:

a buffer layer between the high-k material layer and the gate electrode.

7. The semiconductor device of claim 6, wherein the buffer layer comprises one of TiN, HfN, TaN, ZrN, LaN, SiN, and TiSi.

8. The semiconductor device of claim 6, wherein the buffer layer has a thickness within the range of 10Å to 200Å.

9. The semiconductor device of claim 1, wherein the species comprises one of N, F, Si, O, Hf, Zr, Ti, Ta, Y, V, Sc, Ba, Sr, Ru, B, Al, Ga, In, Ge, C, P, As, and Sb.

10. The semiconductor device of claim 1, wherein the high-k material layer comprises one of HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, SiO_2, SiON, Ta_2O_5, La_2O_3, and AL_2O_3.

11. The semiconductor device of claim 1, wherein the high-k material layer has a thickness within the range of 10Å to 60Å.

12. The semiconductor device of claim 1, wherein the high-k material layer has an equivalent oxide thickness within the range of 3Å to 20Å.

13. The semiconductor device of claim 1, wherein a dose of the implanted species is within the range of $1x10^{13}$ ions/cm^2 to $1x10^{16}$ ions/cm^2.

14. The semiconductor device of claim 1, wherein the isolation regions comprise trench isolation regions.

15. A transistor comprising:

a gate electrode;

a high-k gate dielectric layer implanted with a species, the high-k gate dielectric layer proximate the gate electrode; and

a substrate comprising an active region, the substrate proximate the high-k gate dielectric layer.

16. The transistor of claim 15, further comprising:

a buffer layer between the gate electrode and the high-k gate dielectric layer.

17. The transistor of claim 15, wherein the gate electrode comprises one of aluminum and polysilicon.

18. A method of making a semiconductor comprising:

forming isolation regions, well regions, and active regions on a substrate;

treating a surface of the substrate to form a pre-gate material on the substrate;

depositing a high-k material on the pre-gate material;

performing ion implantation to implant a species into the high-k material; and

depositing a gate electrode material on the high-k material.

19. The method of claim 18, further comprising:

annealing the high-k material.

20. The method of claim 18, further comprising:

depositing a buffer layer on the high-k material.

21. The method of claim 20, wherein depositing the buffer layer comprises depositing one of TiN, HfN, TaN, ZrN, LaN, SiN, and TiSi.

22. The method of claim 20, wherein the buffer layer provides a diffusion reservoir for the ion implantation.

23. The method of claim 20, wherein the buffer layer is deposited using one of atomic layer deposition, metal-organic chemical vapor deposition, plasma vapor deposition, and jet vapor deposition.

24. The method of claim 18, wherein the high-k material is deposited using one of atomic layer deposition, metal-organic chemical vapor deposition, plasma vapor deposition, and jet vapor deposition.

25. The method of claim 18, further comprising:

forming a transistor from the substrate, pre-gate material, high-k material and gate electrode material.

26. The method of claim 18, wherein the ion implantation is performed by using one of a beamline implanter and a plasma implanter.

27. The method of claim 18, wherein the substrate comprises silicon.

28. The method of claim 18, wherein an implant energy of the ion implantation is within the range 5eV to 10keV.

29. The method of claim 18, wherein a dose of the implantation is within the range of $1x10^{13}$ ions/cm^2 to $1x10^{16}$ ions/cm^2.

30. The method of claim 18, wherein depositing the high-k material comprises depositing one of HfO_2, HfSiO, ZrO_2, ZrSiO, SiO_2, SiON, Ta_2O_5, La_2O_3, and AL_2O_3.

31. The method of claim 18, wherein performing ion implantation to implant the species comprises implanting one of N, F, Si, O, Hf, Zr, Ti, Ta, Y, V, Sc, Ba, Sr, Ru, B, Al, Ga, In, Ge, C, P, As, and Sb.

32. The method of claim 18, wherein treating the surface of the substrate to form the pre-gate material comprises forming the pre-gate material comprising one of SiO_2 and SiON.

33. A method for fabricating sub-100nm metal oxide semiconductor field-effect transistor devices comprising:

forming isolation regions and active regions on a substrate;

treating the substrate to form a pre-gate material layer on the substrate;

depositing a high-k material on the pre-gate material;

perfoming ion implantation to implant a species into the high-k material;

depositing a gate electrode material on the high-k material; and

forming a transistor from the substrate, pre-gate material, high-k material, and gate electrode material.

34. A method for fabricating a semiconductor device comprising:

means for treating a surface of a substrate;

means for depositing a high-k material layer on the treated surface;

means for implanting a species into the high-k material; and

means for depositing a gate electrode material layer on the high-k material layer.

35. The method of claim 34, further comprising:

means for depositing a buffer layer on the high-k material layer.

36. The method of claim 34, further comprising:

means for forming a transistor from the substrate, high-k material layer, and gate electrode material layer.

37. A semiconductor device comprising:

a substrate including isolation regions and active regions;

a first high-k material layer implanted with a first species, the first high-k material layer proximate the substrate;

a second high-k material layer implanted with a second species, the second high-k material layer proximate the first high-k material layer; and

a gate electrode proximate the second high-k material layer.

38. The semiconductor device of claim 37, wherein the first high-k material layer comprises one of $HfSiO_x$ and $ZrSiO_x$.

39. The semiconductor device of claim 37, wherein the first species and the second species comprise N.

40. The semiconductor device of claim 37, further comprising:

a third high-k material layer implanted with a third species, the third high-k material layer located between the first high-k material layer and the second high-k material layer.